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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2892	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/989,372	LANE, RICHARD H.	
	Examiner	Art Unit	
	Chuong A. Luu	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/13/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-32,34-39,41,44-47,49 and 51-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *65* is/are allowed.

6)☒ Claim(s) *29-32,34-39,41,44-47,49 and 51-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

WITHDRAWN

The indicated allowability of claim 65 is withdrawn in view of the newly discovered reference(s) to Kirlin et al. (U.S. 5,976928). Rejections based on the newly cited reference(s) follow.

Response to Arguments

Applicant's arguments with respect to claims 36-39, 41, 44-47, 49 and 51-65 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claims 55-56 and 65 are rejected under 35 U.S.C. 102(e) as being anticipated by Kirlin et al. (U.S. 5,976928).

Kirkin discloses a capacitor with

(55) a lower electrode provided fully within a first insulating layer (22), said lower electrode (30) comprising an electropolished patterned metal layer having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom;

a second insulating layer (32) provided over said electropolished patterned metal layer and in contact with said first insulating layer (22);

an upper electrode (34) provided over said second insulating layer (34);

(56) wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides (see column 10, lines 5-23);

(65) an insulating layer (22) provided over a substrate (10), the insulating layer (22)including a contact opening (24), the contact opening having a first height;

a barrier conductive layer (28) provided within the contact opening (240, the barrier conductive layer (28) being disposed along a bottom and sidewalls of the contact opening (24), wherein the barrier conductive layer (28) has a first thickness and wherein a length of upwardly extending portions of the barrier conductive layer (28) that are disposed along the sidewalls of the contact opening (24) is equal to the first height;

a lower platinum electrode (30) provided over the barrier conductive layer (28), the lower platinum electrode (30) being disposed along a bottom portion and sidewall portions of the barrier conductive layer (28), wherein a length of upwardly extending portions of the lower platinum electrode (30) that are disposed along the sidewall

portions of the barrier conductive layer (28) is equal to the first height minus the first thickness;

a dielectric layer (32) provided over the lower platinum electrode (30), the dielectric layer (32) being disposed along a bottom portion and sidewall portions of the lower platinum electrode (30) and on an upper surface of the barrier conductive layer (28) and an upper surface of the substrate;

a second platinum electrode (34) provided over the dielectric layer (32), the second platinum electrode (34) being disposed along a bottom portion, sidewall portions and an upper surface of the dielectric layer (32) (see column 10, lines 5-23. Figures 1A-1E).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 29-32 and 34-39, 41, 44-47, 49 and 51--64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirlin et al. (U.S. 5,976928).

Kirlin discloses a capacitor with

(29) a substrate (10); an insulating layer (22) provided over said substrate (10);

an electropolished patterned metal layer (30) provided within an opening (24) of said insulating layer (22), wherein said electropolished metal layer (30) and wherein a top surface of said electropolished metal layer (30) is electropolished down to said insulating layer (22) so that said top surface of said electropolished metal layer (30) is at the same level with a top surface of said insulating layer (22);

a photoresist plug (35) provided within said opening (24) and over and in contact with said electropolished patterned metal layer (30) (see Figures 1C-1E);

(30); (37); (45) wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides (see column 10, lines 5-23);

(31); (38); (46) wherein said electropolished patterned metal layer contains a noble metal (see column 10, lines 5-23);

(32); (39); (47) wherein said electropolished patterned metal layer is a platinum layer (see column 10, lines 5-23);

(35) wherein said electropolished patterned metal layer forms a lower capacitor electrode of said semiconductor device (see Figure 1C-1E);

(36) a transistor including a gate fabricated on a semiconductor substrate (10) and including a source/drain region in said semiconductor substrate (10) disposed adjacent to said gate; an insulating layer provided over said substrate; and a container capacitor including a lower electrode, a dielectric layer over said lower electrode, and an upper electrode over said dielectric layer, said upper electrode comprising doped

polysilicon, and said lower electrode having a surface aligned over said source/drain region, wherein said lower electrode comprises an electropolished patterned metal layer which is situated fully within said insulating layer, wherein said electropolished patterned metal layer, and wherein said dielectric layer is in contact with said insulating layer (see Figure 1C-1E);

(44) a processor; an integrated circuit coupled to said processor, at least one of said integrated circuit and said processor comprising a container capacitor provided within an insulating layer, said container capacitor including a lower electrode and an upper electrode, said lower electrode comprising an electropolished patterned metal layer, wherein a top surface of said electropolished patterned metal layer is at the same level with a top surface of said insulating layer such that said lower electrode does not extend above the top surface of said insulating layer, and said upper electrode comprising doped polysilicon (see Figure 1C-1E);

(51) wherein said integrated circuit is a memory module (see Figure 1C-1E);

(52) wherein said memory module is a DRAM memory (see column 7, lines 42-44);

(53) wherein said memory module is a SRAM memory (see Figure 1C-1E);

(54) wherein said memory module is a MCM memory (see Figure 1C-1E);

(59) an insulating layer provided over a substrate, said insulating layer containing an opening; a tantalum nitride barrier conductive layer provided at a bottom of said opening; a lower electrode provided over said tantalum nitride barrier conductive layer, said lower electrode comprising an electropolished patterned metal layer having a

bottom and vertical sidewalls extending upwardly from said bottom such that said lower electrode is situated fully within said insulating layer, said lower electrode; a dielectric material provided over said electropolished pattemed metal layer and in contact with said insulating layer; an upper electrode comprising doped polysilicon provided over said dielectric material and wherein said lower electrode, said dielectric material and said upper electrode form said container capacitor (see Figure 1C-1E);

(60) an insulating layer provided over a substrate; a opening provided in said insulating layer; a plurality of lower capacitor electrodes provided along the bottom and sidewalls of respective ones of said openings, said lower electrodes being formed as discrete electropolished metal layers such that said lower electrodes do not extend above an upper surface of said insulating layer; and a dielectric layer associated with each of said discrete lower electrodes, said dielectric layer being in contact with said insulating layer (see Figure 1C-1E);

(61) wherein said capacitor structure further comprises an upper electrode associated with each of said discrete lower electrodes (see Figure 1C-1E);

(64) wherein said lower capacitor electrodes contain platinum (see column 10, lines 5-23).

Kirlin teaches the above outlined features except for describing the thicknesses of the metal layer approximately 50-300Å and a plurality of openings. Even through, Kirlin does not explicitly disclose the thicknesses of the metal layer approximately 50-300Å. However, the thicknesses of the metal layer approximately 50-300Å is considered to be obvious. Therefore, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to modify the teaching of Kirlin since it has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. Also, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. In re Leshin, 125 USPQ 416 and In re Aller, 105 USPQ 233 (see MPEP 2144.05). St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chuong A Luu/
Primary Examiner, Art Unit 2892
June 09, 2008